IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: ITO et al.	Atty. Dkt.: 01-560
Serial No.: 10/786,136	Art Unit: 2123
Filed: 2/26/2004	Examiner: Janakiraman
Title: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND MICROCOMPUTER DEVELOPMENT ASSISTING APPARATUS	

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Date: 14 July 2008

APPEAL BRIEF UNDER 37 CFR §41.31

Sir:

The appellants hereby submit one copy of a Brief on Appeal under 37 C.F.R. §41.31. A Notice of Appeal was filed on May 16, 2008.

1. REAL PARTY IN INTEREST

The real party in interest is DENSO CORPORATION, the assignee of record, as evidenced by the assignment recorded at reel/frame 015025/0987.

2. RELATED APPEALS AND INTERFERENCES

There is no known related appeal or interference that will directly affect, that will be directly affected by, or that will have a bearing on the Board's decision on this appeal.

3. STATUS OF CLAIMS

Claims 1-16 stand finally rejected as noted in the final office action mailed on December 19, 2007 and maintained in the Advisory Action mailed on April 25, 2008. The rejection of claims 1-16 is now being appealed.

4. STATUS OF AMENDMENTS

No amendments to the claims were filed subsequent to the final rejection. An Amendment under 37 CFR 1.116 was filed on March 19, 2008 after the final rejection; however, the Amendment did not include claim amendments.

5. SUMMARY OF CLAIMED SUBJECT MATTER

In the following summary, parts of the claims are corresponded with reference numbers from the illustrated embodiments for ease of understanding.

Claim 1

Claim 1 is directed to a semiconductor integrated circuit device (FIG. 1, element 14) for emulating operation of a one-chip microcomputer having a CPU (FIG. 1, element 22) and a peripheral circuit (e.g., FIG. 1, element 23) that is controlled by the CPU (22) (FIG. 1; page 5, lines 22-24). Further referring to the illustrated embodiment shown in FIG. 1, the device comprises a vector address switching circuit (28; page 7, lines 10-12) and an interface circuit (18; page 5, line 26 to page 6, line 1). The vector address switching circuit (28) is configured for outputting a vector address corresponding to a reset vector address supplied from the CPU (22) when receiving a first reset signal (RST1), and for outputting a prescribed vector address instead of the vector address corresponding to the reset vector address supplied from the CPU (22) when receiving a second reset signal (RST2) (page 8, lines 8-22). The interface circuit (18) is configured for performing input and output of information relating to emulation between the CPU (22) and an external circuit (page 5, line 26 to page 6, line 3). The CPU (22) is configured to execute different programs depending on the vector address and the prescribed vector address output from the vector address switching circuit (page 9, lines 13-20). The CPU (22) is constructed to be reset by the first and second reset signals (RST1, RST2; page 8, lines 17-19), and the interface circuit (18) is constructed to be reset by the second reset signal (RST2) but not by the first reset signal (RST1) (page 8, lines 20-22).

Claim 9

Independent claim 9 is directed to a microcomputer development assisting apparatus (FIG. 1, element 11; page 5, lines 11-14). As illustrated for example in FIG. 1, the microcomputer development assisting apparatus (11) comprises a semiconductor integrated circuit device (14) for emulating operation of a one-chip microcomputer having a CPU (22) and a peripheral circuit (23) that is controlled by the CPU (22) in a state that the semiconductor integrated circuit device (14) is electrically connected, in place of the one-chip microcomputer, to a circuit board (12) to be mounted with the one-chip microcomputer; and a host (17). The host (17) is for setting a condition of emulation by the semiconductor integrated circuit device (14) and for performing data processing on an emulation result.

The semiconductor integrated circuit device (14) includes a CPU (22); a peripheral circuit (23) that is controlled by the CPU; a vector address switching circuit (28); and an interface circuit (18). The vector address switching circuit (28) is for outputting a vector address of a user program corresponding to a reset vector address supplied from the CPU (22) when receiving a first reset signal (RST1) from the circuit board (12), and for outputting a vector address of a monitor program instead-of the vector address corresponding to the reset vector address supplied from the CPU (22) when receiving a second reset signal (RST2) from the host. (17) (page 8, lines 8-22). The interface circuit (18) is for performing input and output of information relating to the emulation between the CPU (22) and an external circuit (page 5, line 26 to page 6, line 3). The CPU (22) is configured to execute different programs depending on the vector address and the prescribed vector address output from the vector address switching circuit (page 9, lines 13-20). The CPU (22) is constructed to be reset by the first and second reset signals (RST1, RST2; page 8, lines 17-19), and the interface circuit (18) is constructed to be reset by the second reset signal (RST2) but not by the first reset signal (RST1).

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-16 are anticipated under 35 USC 102(e) by U.S. Patent No. 6,877,112, Iino ("Iino").

7. ARGUMENT

A. Claims 1-16 are not anticipated under 35 USC 102(e) by U.S. Patent No. 6,877,112, Iino ("Iino").

The Iino reference fails to disclose each and every one of the claim limitations, as explained in more detail below. Therefore, this rejection should be reversed.

Claims 1-8

One aspect of the application mentions solving the problem of "correctly emulating an operation to be performed immediately after generation of a reset signal." (Specification page 3, lines 7-10.)

Claim 1 recites in combination, for example "a vector address switching circuit configured for outputting a vector address corresponding to a reset vector address supplied from the CPU when receiving a first reset signal, and for outputting a prescribed vector address instead of the vector address corresponding to the reset vector address supplied from the CPU when receiving a second reset signal; and an interface circuit configured for performing input and output of information relating to emulation between the CPU and an external circuit, wherein the CPU is configured to execute different programs depending on the vector address and the prescribed vector address output from the vector address switching circuit, and wherein the CPU is constructed to be reset by the first and second reset signals, and the interface circuit is constructed to be reset by the second reset signal but not by the first reset signal." Accordingly, the vector address switching circuit causes the CPU to execute different programs in accordance with different (first or second) reset signals, whereas the interface circuit is reset only by the second reset signal.

The office actions assert that Iino, FIGs. 3 and 4-5 discloses the invention as claimed. To the contrary, Iino fails to set forth each and every element found in the claims. "A claim is

anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Furthermore, the elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

As stated in the first office action, Iino is directed to a reset control system and method. The first and final office actions cite Iino, column 2, lines 55-67 and column 3, lines 1-6 (referring to Iino FIG. 3) as teaching the vector address switching circuit. According to Iino, FIG. 3, the first reset control section (605) OR-operates first and second reset signals; the OR operation result is output to the CPU core (604) as a first internal reset signal (629) for initializing the CPU core (604) (column 3, lines 55-63). A companion chip (606) has a second reset control section (607) that distributes the external reset signal (626) to a second internal reset signal (627) and second reset signal (628). (Col. 2, line 64 to Col. 3, line 2.)

Iino fails to teach or suggest, for example, the vector address switching circuit as further recited in claim 1. The final office action, page 3, last line to page 4, first line refers to Iino, column 2, lines 55-67 and column 3, lines 1-6 (discussing Iino FIG. 3; Iino states that FIG. 3 is prior art) as teaching first and second reset signals and executing different programs (user and monitor) by outputting different vector addresses of programs in correspondence to the reset signals; and column 11, lines 43-47 (discussing Iino's own device, FIG. 5) as teaching well known art regarding reset signals. The examiner explained during the interview of March 19, 2008 that the combination of first and second reset signals in Iino, FIG. 3 is considered to

correspond to the recited "vector address switching circuit" which outputs different vector addresses to the CPU.

In Iino column 2, lines 55-67 (relied on in the final office action, page 3), two reset signals 526, 528 are applied to and OR-operated by a control section 605 (col. 3, lines 36-39), which in turn resets a CPU 604 by a single reset signal 629. This corresponds to two reset signals RST1, RST2 and an OR circuit 31, which reset CPU 22, illustrated in FIG. 1 of the present application. In each of Iino's cases, it is only possible to reset the CPU, and the CPU starts the same program. Iino's CPU cannot recognize which one of the different reset signals is used, and hence cannot differentiate "different programs" to execute after being thus reset. Accordingly, the examiner's contention in the final office action that the reset signal causes different addresses to be loaded to change different programs is incorrect and certainly is not "well-known".

According to independent claim 1, besides the above-discussed reset operation, a "vector address switching circuit" is configured to output different vector addresses ("vector address" or "prescribed vector address") to the CPU, corresponding respectively to the different reset signals RST1, RST2. Consequently, the CPU is enabled to recognize which one of the different reset signals is resetting it, and will execute different programs by referring to the different respective vector addresses.

Iino also fails to teach or suggest that "the CPU is configured to execute different programs depending on the vector address and the prescribed vector address output from the vector address switching circuit." The Advisory Action contends that Iino's "first reset control section 13 generates a first processor internal reset signal 111 and outputs it to the CPU core section 12" corresponds to "outputting a vector address corresponding to a reset vector address"

(Advisory Action page 2, third paragraph). To the contrary, the execution of different programs (e.g., user program, monitor program) depending on the ***vector address*** output from the switching circuit is different from simply resetting. That is, a reset without more merely restarts the same program.

Hence, Iino absolutely fails to teach or suggest, for example, "***a vector address switching circuit*** configured for outputting ***a vector address corresponding to a reset vector address supplied from the CPU when receiving a first reset signal***, and for outputting ***a prescribed vector address instead of the vector address corresponding to the reset vector address supplied from the CPU when receiving a second reset signal.***" (See, e.g., claim 1.) To the contrary, although Iino discloses different reset signals, Iino fails to teach or suggest anything about outputting different vector addresses from a vector address switching circuit to selectively switch based on the reset signal to different programs to be executed by a CPU.

The Advisory Action dismisses the appellants' arguments concerning Iino, column 2, lines 55-67 and column 3, lines 1-6, and FIG. 3 (discussed above) as being improperly directed to Iino's admitted prior art rather than Iino's own device. These portions of Iino are properly addressed because they are relied upon in the rejection in the final office action as teaching the recited vector address switching circuit. Accordingly, the appellants continue to maintain that the examiner's observations about Iino, column 2, lines 55-67 and column 3, lines 1-6 are incorrect. To the extent that the examiner is relying on a combination of Iino's prior art device (either FIG. 1, 2 or 3) and Iino's device (e.g., FIGs. 4-6), the rejection under 35 USC 102(e) must be withdrawn, since "The ***identical invention*** must be shown in as complete detail as is contained in the ... claim." (*Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (emphasis added)) and the elements must be arranged as required by

the claim (*In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)). It is improper for the examiner to rely on a combination of two different devices in an anticipation rejection.

Iino also fails to teach or suggest the interface circuit as recited in the last wherein clause in claim 1: "wherein ... the interface circuit is constructed to be reset by the second reset signal but not by the first reset signal." Iino, FIG. 4 discloses the resetting of a CPU 12 by a reset control section 13. Specifically, Iino's CPU 12 is power-on reset by a first reset signal 109, 111 and hard-reset by a second reset signal 110, 112. (Column 6, lines 9-16.) This is somewhat analogous to the first part of the last "wherein" clause recited in claim 1: "the CPU is constructed to be reset by the first and second reset signals". Iino, however, fails to teach or suggest the interface circuit as recited in the remainder of the last "wherein" clause: "the interface circuit is constructed to be reset by the second reset signal but not by the first reset signal."

The final office action considers the interface circuit to be taught by Iino, column 1, lines 26-27 (the office action's reference to column "2" is a typographical error), referring to Iino FIG. 1. Iino FIG. 1 is labeled as "prior art" and is a different device from Iino's device shown in FIG. 4-6 and principally relied on by the office action. To the extent that the examiner is relying on a combination of Iino's prior art device (FIG. 1) and Iino's device (e.g., FIGs. 4-6), the rejection under 35 USC 102(e) must be withdrawn, since "the identical invention must be shown in as complete detail as is contained in the ... claim" (*Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)) and the elements must be arranged as required by the claim (*In re Bond,* 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)).

The final office action states that the recitation "the interface circuit is constructed to be reset by the second reset signal but not by the first reset signal" (claim 1) "is the definition of reset signals" (final office action, page 4, line 13). This holding is respectfully traversed, since

there is no such definition of record, and in any event Iino FIG. 1 (considered by the examiner to have an interface circuit to the emulator 401) does not have an interface circuit which is reset by the second but not the first reset signal, thereby showing that such recitation is not the "definition of reset signals."

Iino fails to teach or suggest, for example, these elements recited in amended independent claim 1. Claims 2-8 depend directly or indirectly from claim 1 and are deemed to be patentable over the references for reasons including those provided above. It is respectfully submitted therefore that claims 1-8 are patentable over Iino.

Claims 9-16

Claims 9-16 are deemed by the office actions to be anticipated by Iino for the identical reasons as claims 1-8, respectively. Each of the arguments presented above with regard to claims 1-8 are hereby incorporated by reference, but will not be expressly repeated to avoid obscuring the issues.

It is respectfully submitted that claims 9-16 are not anticipated by Iino for the reasons provided above. Claims 9-16 are further deemed to be not anticipated by Iino for the following additional reason.

Independent claim 9 recites "a host for setting a condition of emulation by the semiconductor integrated circuit device and for performing data processing on an emulation result." None of the office actions has explicitly addressed this limitation. That is, at least one element in independent claim 9 is completely ignored by the office actions and consequently there is no *prima facie* case of anticipation with regard to claim 9.

Iino fails to teach or suggest, for example, these elements recited in independent claim 9. Claims 10-16 depend directly or indirectly from claim 9 and are deemed to be patentable over

the references for reasons including those provided above. It is respectfully submitted therefore that claims 9-16 are patentable over Iino.

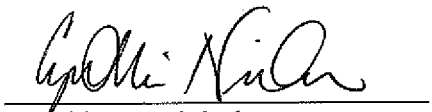
Summary

For at least these reasons, the combination of features recited in independent claims 1 and 9, when interpreted as a whole, is submitted to patentably distinguish over the references of record. Therefore, the rejection of claim 1-16 should be reversed.

In summary, based on the comments above, the appellants respectfully submit that claims 1-16 are not anticipated by Iino. The Examiner's rejection of claims 1-16 on these grounds is therefore improper and should be reversed.

If there are any problems with the payment of fees, please charge any underpayments and credit any overpayments to Deposit Account No. 01-0305.

Respectfully submitted,



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8. CLAIMS APPENDIX

1. A semiconductor integrated circuit device for emulating operation of a one-chip microcomputer having a CPU and a peripheral circuit that is controlled by the CPU, the device comprising:

a vector address switching circuit configured for outputting a vector address corresponding to a reset vector address supplied from the CPU when receiving a first reset signal, and for outputting a prescribed vector address instead of the vector address corresponding to the reset vector address supplied from the CPU when receiving a second reset signal; and

an interface circuit configured for performing input and output of information relating to emulation between the CPU and an external circuit,

wherein the CPU is configured to execute different programs depending on the vector address and the prescribed vector address output from the vector address switching circuit, and

wherein the CPU is constructed to be reset by the first and second reset signals, and the interface circuit is constructed to be reset by the second reset signal but not by the first reset signal.

2. The semiconductor integrated circuit device according to claim 1, wherein:

the peripheral circuit includes a functional circuit for realizing a primary function of the peripheral circuit, a stop control circuit for stopping, in response to reception, by the CPU, of a break request that has occurred during execution of an instruction by the CPU, progress of an operation of the functional circuit until completion of processing that is performed in response to the break request, and a setting information storage circuit for storing setting information indicating whether to enable or disable an operation stop function of the stop control circuit; and

the functional circuit of the peripheral circuit is constructed to be reset by the first and second reset signals, and the stop control circuit and the setting information storage circuit are constructed to be reset by the second reset signal but not by the first reset signal.

3. The semiconductor integrated circuit device according to claim 1, further comprising:

an emulation memory for storing a user program that is executed by the CPU in response to the first reset signal; and

a monitor program memory for storing a monitor program that is executed by the CPU in response to the second reset signal.

4. The semiconductor integrated circuit device according to claim 1, wherein:

the CPU is operable in an normal operation mode and a low power consumption operation mode that is lower in power consumption than the normal operation mode; and

a break request control circuit is provided for causing a transition of the CPU to a break state after input of a wake-up signal for returning the CPU from the low power consumption operation mode to the normal operation mode when a break request signal is input externally in a period when the CPU is in the low power consumption operation mode.

5. The semiconductor integrated circuit device according to claim 4, wherein the break request control circuit is constructed to immediately output a break request signal to the CPU if the break request signal is input in a period when the CPU is in the normal operation rode, and outputs a break request signal to the CPU upon input of the wake-up signal if the break request signal is input in a period when the CPU is in the low power consumption operation mode.

6. The semiconductor integrated circuit device according to claim 4, further comprising:

a break request control register that is reset by the second reset signal,

wherein the break request control circuit is constructed to cause a transition of the CPU to the break state immediately or after input of the wake-up signal when the break request signal is input externally in a period when the CPU is in the low power consumption operation mode depending on a value of the break request control register.

7. The semiconductor integrated circuit device according to claim 4, further comprising:

a wake-up signal generation circuit for generating awake-up signal when a prescribed set time has elapsed from a transition of the CPU from the normal operation mode to the low power consumption operation mode.

8. The semiconductor integrated circuit device according to claim 7, wherein the wake-up signal generation circuit includes:

a counter for performing a counting operation in a period when the CPU is in the low power consumption operation mode;

a storage circuit for storing a set count corresponding to the set time; and

a comparator circuit for comparing a value of the counter with the set count of the storage circuit, and for outputting the wake-up signal when the value of the counter has reached the set count.

9. A microcomputer development assisting apparatus comprising:

a semiconductor integrated circuit device for emulating operation of a one-chip microcomputer having a CPU and a peripheral circuit that is controlled by the CPU in a state that the semiconductor integrated circuit device is electrically connected, in place of the one-chip microcomputer, to a circuit board to be mounted with the one-chip microcomputer; and

a host for setting a condition of emulation by the semiconductor integrated circuit device and for performing data processing on an emulation result,

wherein the semiconductor integrated circuit device includes

a CPU;

a peripheral circuit that is controlled by the CPU;

a vector address switching circuit for outputting a vector address of a user program corresponding to a reset vector address supplied from the CPU when receiving a first reset signal from the circuit board, and for outputting a vector address of a monitor program instead-of the vector address corresponding to the reset vector address supplied from the CPU when receiving a second reset signal from the host, and

an interface circuit for performing input and output of information relating to the emulation between the CPU and an external circuit,

wherein the CPU is configured to execute different programs depending on the vector address and the prescribed vector address output from the vector address switching circuit, and

wherein the CPU is constructed to be reset by the first and second reset signals, and the interface circuit is constructed to be reset by the second reset signal but not by the first reset signal.

10. The microcomputer development assisting apparatus according to claim 9, wherein:

the peripheral circuit includes a functional circuit for realizing a primary function of the peripheral circuit, a stop control circuit for stopping, in response to reception, by the CPU, of a break request that has occurred during execution of an instruction by the CPU, progress of an operation of the functional circuit until completion of processing that is performed in response to

the break request, and a setting information storage circuit for storing setting information indicating whether to enable or disable an operation stop function of the stop control circuit; and

the functional circuit of the peripheral circuit is constructed to be reset by the first and second reset signals, and the stop control circuit and the setting information storage circuit are constructed to be reset by the second reset signal but not by the first reset signal.

11. The microcomputer development assisting apparatus according to claim 9, wherein the semiconductor integrated circuit device further includes:

an emulation memory for storing a user program that is executed by the CPU in response to the first reset signal; and

a monitor program memory for storing a monitor program that is executed by the CPU in response to the second reset signal.

12. The microcomputer development assisting apparatus according to claim 9, wherein:

the CPU is operable in an normal operation mode and a low power consumption operation mode that is lower in power consumption than the normal operation mode; and

the semiconductor integrated circuit device further includes a break request control circuit for causing a transition of the CPU to a break state after input of a wake-up signal for returning the CPU from the low power consumption operation mode to the normal operation mode when a break request signal is input externally in a period when the CPU is in the low power consumption operation mode.

13. The microcomputer development assisting apparatus according to claim 12, wherein the break request control circuit is constructed to immediately output a break request signal to the CPU if the break request signal is input in a period when the CPU is in the normal operation

mode, and outputs a break request signal to the CPU upon input of the wake-up signal if the break request signal is input in a period when the CPU is in the low power consumption operation mode.

14. The microcomputer development assisting apparatus according to claim 12, wherein:

the semiconductor integrated circuit device further includes a break request control register that is reset by the second reset signal; and

the break request control circuit is constructed to cause a transition of the CPU to the break state immediately or after input of the wake-up signal when the break request signal is input externally in a period when the CPU is in the low power consumption operation mode depending on a value of the break request control register.

15. The microcomputer development assisting apparatus according to claim 12, wherein the semiconductor integrated circuit device further includes a wake-up signal generation circuit for generating a wake-up signal when a prescribed set time has elapsed from a transition of the CPU from the normal operation mode to the low power consumption operation mode.

16. The semiconductor integrated circuit device according to claim 15, wherein the wake-up signal generation circuit includes:

a counter for performing a counting operation in a period when the CPU is in the low power consumption operation mode;

a storage circuit for storing a set count corresponding to the set time; and

a comparator circuit for comparing a value of the counter with the set count of the storage circuit, and for outputting the wake-up signal when the value of the counter has reached the set count.

9. EVIDENCE APPENDIX

[None]

10. RELATED PROCEEDINGS APPENDIX

[None]